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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,645	02/06/2002	Scot A. Kellar	219.40606X00	4506

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ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

EXAMINER	
BEREZNY, NEMA O	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 10/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/066,645	KELLAR ET AL.	
	Examiner	Art Unit	
	Nema O Berezny	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11,13-17 and 19-26* is/are pending in the application.

4a) Of the above claim(s) *1-7* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-11,13-17 and 19-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Specification

Cancellation of claims 12 and 18 in Amendment A, filed 6-30-03 is acknowledged.

Claim Objections

Claim13 is objected to because of the following informalities: Claim 13 depends from claim 1 which is a non-elected withdrawn claim. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 8-9, 11, 13-15, 17, and 19-22, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta et al. (2002/0163072) in view of Barth et al. (2003/0003703) and Forouhi et al. (2003/0053081). Gupta discloses a three-dimensional (3-D) integrated chip system, comprising: a first wafer (Figs.2-10 el.202) including one or more integrated circuit (IC) devices (el.112), metallic lines (el.210) deposited via an interlevel dielectric (ILD) and settled on the surface higher than the ILD (el.113,116; Fig.7) for wafer-to-wafer bonding and electrical

interconnection, and an ILD recess surrounding the metallic lines deposited via the ILD (Fig.7); and a second wafer (el.100) including one or more integrated circuit (IC) devices (el.112), metallic lines (el.132) deposited via an interlevel dielectric (ILD) and settled on the surface higher than the ILD (el.113,116; Fig.7) for wafer-to-wafer bonding and electrical interconnection, and an ILD recess surrounding the metallic lines deposited via the ILD (Fig.7), wherein the metallic lines on the surface of the second wafer are bonded with the metallic lines on the surface of the first wafer to facilitate direct metal bonding between the first and second wafers to establish electrical connections between active IC devices on the adjacent wafers (Fig.8; p.3 para.29-30). Gupta also discloses wherein the metallic lines include Copper (Cu) bonding pads deposited on opposing surface of the adjacent wafers to serve as electrical contacts between active IC devices on both the adjacent wafers (p.3 para.29); wherein the ILD recess is created by selectively etching the ILD surrounding the metallic lines deposited via the ILD (p.3 para.29); and wherein the first wafer is thinner than the second wafer to conform to height differences of the metallic lines across opposing surfaces of the adjacent wafers (p.3 para.31).

Gupta does not disclose a high temperature deformable interlayer dielectric, or a SiLK dielectric. However, Barth discloses wherein the ILD is a high-temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded, and wherein the high -temperature deformable dielectric is SILK which exhibits a glass transition near 450 degrees C while the metallic lines exhibit a bonding temperature of about 400 degrees

C (p.2 para.18-19). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the SiLK dielectric of Barth with the IC system of Gupta. SiLK dielectric has energy band gaps and extinction coefficients that are sensitive indicators of the curing temperature and time for the curing process (Forouhi - p.1 para.10).

Claims 10, 16, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gupta in view of Barth and Forouhi as applied to claims 8-9, 11, and 13-15 above, and further in view of Desai et al. (5,656,554). Gupta in view of Barth and Forouhi do not disclose wherein the ILD recess is created by a Chemical Mechanical Polish (CMP). However, Desai discloses controlling the solution of a CMP slurry wherein a surrounding dielectric material would be polished or removed at a faster rate than a center conductive/metallic plug (col.4 lines 9-15, 20-38; col.5 lines 6-15). Therefore, it would have been obvious to a person skilled in the art at the time of the invention to use the CMP slurry and procedure of Desai with the IC system of Gupta, Barth, and Forouhi in order to avoid overpolishing or dishing a conductive plug surrounded by dielectric material.

Response to Arguments

Applicant's arguments filed 6-30-03 have been fully considered but they are not persuasive. Even though all of the prior claims have been amended, claims 8 and 14 have been rewritten to incorporate all of the limitations of cancelled claims 12 and 18,

respectively. Therefore, Applicant's arguments regarding amended claims 8 and 14 will be addressed.

Applicant contends that Barth does not disclose a high temperature deformable dielectric used to allow the bonding areas to be self-leveling to account for height variations across the adjacent wafers to be bonded, or that such a high-temperature deformable dielectric is SILK which exhibits a glass transition near 450 degrees while the metallic lines exhibit a bonding temperature of about 400 degrees, as claimed. Examiner disagrees. Applicant's specification states on page 11 lines 4-19 that when copper metal lines on a wafer or substrate use SILK dielectric as an interlevel dielectric, said dielectric will plastically deform to allow the bond pads to be self-leveling to account for height variations; said specification also states that SILK has a glass transition temperature of 450 degrees C while copper metal lines bond at 400 degrees C. As stated in the prior and instant rejections, Gupta in view of Barth and Forouhi disclose copper metal lines in a SILK interlevel dielectric. Therefore, since the conditions for Barth are the same as those disclosed by Applicant, then the results of a self-leveling dielectric, and the temperature differences for said dielectric and the metal lines would have occurred for Barth also.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nema O Berezny whose telephone number is (703) 305-3445. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on (703) 308-4940. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

NB

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800